Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-26. (canceled).

27. (currently amended) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate;

implanting a field implant;

implanting a well implant;

implanting an enhancement implant;

forming a gate oxide on the semiconductor substrate;

forming a gate on the gate oxide;

implanting a first pocket implant into the semiconductor substrate from a first side of the gate; and

implanting a second pocket implant into the semiconductor substrate from a second side of the gate; and

diffusing the first pocket implant and the second pocket implant laterally in the semiconductor substrate to form a non-uniform dopant concentration throughout a channel region, the non-uniform dopant concentration is configured to increase a punch-through voltage immunity threshold, and

~~;and further doping the first pocket implant and the second pocket implant with a blanket implant,~~

wherein the first pocket implant and the second pocket implant are in contact at about the center of ~~a~~ the channel region.

28. (canceled).

29. (previously presented) The method of claim 27 wherein the first pocket implant and the second pocket implant are implanted at an angle.

30. (previously presented) The method of claim 27 wherein the first pocket implant and the second pocket implant are implanted using the gate as a mask.

31. (currently amended) The method of claim 27 wherein the diffusing comprises a non-uniform diffusion configured to optimize ~~increases~~ a reverse short channel effect of the transistor.

32. (canceled).

33. (previously presented) The method of claim 27 further comprising forming a source on the first side of the gate and a drain on the second side of the gate, wherein the source and drain are doped at a first polarity and the first pocket implant and the second pocket implant are doped at a second polarity.

34. (previously presented) The method of claim 33 wherein the first polarity is different than the second polarity.

35. (currently amended) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate;

forming a gate oxide on the semiconductor substrate;

forming a gate on the gate oxide;

implanting a first pocket implant and a second pocket implant into the semiconductor substrate using the gate as a mask; and

diffusing the first and second pocket implants laterally causing the first pocket implant to merge with the second pocket implant at about a center portion of a channel disposed therebetween, the first and second pocket implants being diffused non-uniformly across the

channel to adjust the punch-though voltage immunity~~, wherein the first and second pocket implants are further doped with a blanket implant~~.

36. (currently amended) The method of claim 35 wherein the diffusing comprises providing a non-uniform diffusion to optimize ~~increases~~ a reverse short channel effect of the transistor.

37. (previously presented) The method of claim 35 further comprising implanting an enhancement implant in the semiconductor substrate.

38. (currently amended) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate having a surface;

forming a gate oxide on the semiconductor substrate surface;

forming a gate on the gate oxide;

implanting a first pocket implant into the semiconductor substrate from a first side of the gate at an angle;

implanting a second pocket implant into the semiconductor substrate from a second side of the gate at an angle; and

diffusing the first and second pocket implants laterally causing the first pocket implant to merge with the second pocket implant; wherein the first and second pocket implants are diffused non-uniformly across a channel region formed therebetween, and wherein the non-uniform diffusion is configured to increase the punch-through voltage threshold ;

~~wherein the first and second pocket implants are further doped with a blanket implant~~.

39. (canceled).

40. (previously presented) The method of claim 38 wherein the first pocket implant and the second pocket implant are implanted using the gate as a mask.

41. (canceled).

42. (currently amended) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate having a surface;

forming a gate oxide on the semiconductor substrate surface;

forming a gate on the gate oxide;

implanting a first pocket implant into the semiconductor substrate from a first side of the gate at an angle;

implanting a second pocket implant into the semiconductor substrate from a second side of the gate at an angle; and

diffusing the first and second pocket implants laterally; wherein the first and second pocket implants are diffused non-uniformly across a channel region formed therebetween, and wherein the non-uniform diffusion is configured to increase a threshold voltage of the transistor ~~,wherein the first and second pocket implants are further doped with a blanket implant~~.

43. (currently amended) The method of claim 42 wherein the diffusing comprises providing a non-uniform diffusion to ~~increases~~ about maximize ~~a~~ the threshold voltage of the transistor relative to the length of the channel region.

44. (previously presented) The method of claim 42 further comprising implanting an enhancement implant in the semiconductor substrate.

45-47. (canceled).

48-52. (canceled).

Please add the following new claims:

53. (new) The method of claim 27 wherein the channel region comprises a boron dopant configured to increase the punch-though voltage immunity.

54. (new) The method of claim 27 wherein the diffusing comprises maximizing the punch-through voltage immunity by adjusting the lateral diffusement of the first pocket implant and the second pocket implant relative to the channel region length such that a maximum threshold voltage is obtained.

55. (new) The method of claim 27 wherein the first pocket implant comprises an n-type of material.

56. (new) The method of claim 55 wherein the first pocket implant comprises phosphorus, arsenic, and combinations thereof.

57. (new) The method of claim 27 wherein the second pocket implant comprises an n-type of material.

58. (new) The method of claim 57 wherein the second pocket implant comprises phosphorus, arsenic, and combinations thereof.